REMARKS

Claims 1-6, 8-12, and 14-20 are cancelled, claims 13, 21, 31, 34, and 35 amended, and claims 41-53 added. Claims 13, 21-26, and 28-53 are pending, where claims 13, 21, 31, 34, 35, 41, and 50 are independent claims. The Applicant has carefully and thoughtfully considered the Office Action and the comments therein. For the reasons given below, it is submitted that this application is in condition for allowance.

1. In the Office Action on page 5 in section 5, the Examiner states that claims 13 and 34 are allowed. The Applicant thanks the Examiner for allowing these claims.

2. In the Office Action on pages 2-5 in section 2, claims 1-6, 8-12, 14-26, 28-33, and 35-40 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 4,575,844 to Kosuge et al. Claims 1-6, 8-12, and 14-20 are cancelled rendering these rejections moot. The Applicant respectfully traverses the remaining rejections.

The invention of the application, as defined by certain of the claims, teaches a switching mechanism where TDM and packet data can be switched by a single shared memory mechanism such that switching packet data has no latency or jitter effect on the TDM traffic. See, e.g., specification, page 5, 14-24. In an exemplary embodiment of the invention not necessarily recited in the claims, TDM and packet shared memory partitions and packet data queues per port contribute to the lack of latency or jitter effect on the TDM traffic. A varying amount of the single shared memory is used to store packet data, whereas the TDM portion of the shared memory is constant. Additionally, the use of routing information stored as part of a data

exchange unit (DEU) assists in routing packet data. The switching of packet data by the shared memory has no latency or jitter effect on the switching of TDM data by the shared memory.

Amended claim 21 recites a switch to switch TDM data and packet data from input ports to output ports. The switch comprises: a plurality of input ports to receive data, wherein each data comprises either TDM data or packet data; a plurality of output ports to transmit switched data; a single shared memory coupling the input ports to the output ports; a time slot interchange controller coupled to the single shared memory to select addresses in the single shared memory to store TDM data; and a packet switch controller coupled to the single shared memory to select addresses in the single shared memory to store packet data. The single shared memory is adapted to receive sequentially all TDM data and all packet data received from the input ports, store both TDM data and packet data, switch all sequentially received TDM data and packet data received from respective input ports to respective output ports. Switching of any received packet data by the single shared memory has neither latency nor jitter effect on switching of any received TDM data by the single shared memory, and switching of any received TDM data is based on input time slots of the TDM data. The time slot interchange controller is adapted to select an address of the single shared memory for a TDM data based on a time slot of a frame in which the switch received the TDM data. The packet switch controller is adapted to select an address of the single shared memory for a packet data based on routing data embedded in the packet data and based on the input port which received the packet data.

Kosuge teaches a digital switching system in Figure 1 having a hierarchical storage. Referring to Figure 1, the hierarchical storage 10 includes a small-capacity high-speed memory 11, a large-capacity low-speed memory 12, and a file memory 13. Referring to Figure 6, the hierarchical storage 10 additionally includes a circuit switching call program and a packet

switching call program in each of the memories 11, 12, and 13. Kosuge, however, fails to teach at least **three** aspects of claim 21.

First, Kosuge fails to teach a time slot interchange and a packet switch controller coupled to a single shared memory. In rejecting claim 21, the Office Action aligns the recited time slot interchange controller with the circuit switching call program parsed over the memories 11, 12, and 13 in Figure 6 of Kosuge and the recited packet switch controller with the packet switching call program parsed over the memories 11, 12, and 13 in Figure 6 of Kosuge. The circuit switching call program and the packet switching call program of Kosuge, however, are **not coupled to** a single shared memory. Instead, the circuit switching call program is parsed over and **included in** three separate memories 11, 12, and 13, and the packet switching call program is parsed over and **included in** three separate memories 11, 12, and 13. Kosuge, Figure 6; column 28-55. Hence, Kosuge fails to teach a time slot interchange and a packet switch controller coupled to a single shared memory.

Moreover, Kosuge teaches away from being modified such that the circuit switching call program and the packet switching call program are **coupled to** a single shared memory. The hierarchical storage 10 of Kosugue, however, consists of three separate and distinct memories, namely the small-capacity high-speed memory 11, the large-capacity low-speed memory 12, and the file memory 13. Kosuge, Figure 1; column 3, lines 24-27; column 6, lines 8-25. For circuit switching, the small-capacity high-speed memory 11 is used. Kosuge, column 1, lines 64-66; column 3, lines 29-35; column 6, lines 4-8 and 15-18; Figures 4 and 5. For packet switching, the small-capacity high-speed memory 11, the large-capacity low-speed memory 12, and the file memory 13 are used. Kosuge, column 1, lines 64-66; column 3, lines 29-39; column 6, lines 8-14 and 18-25; Figures 4 and 5. Due to the **hierarchical data flow** between the three memories

11, 12, and 13 in the hierarchical storage, Kosuge requires the circuit switching call program and the packet switching call program to be **included in** the three memories 11, 12, and 13 and **not coupled to** a single shared memory. See, Kosuge, column 3, lines 40-55. Hence, Kosuge teaches away from being modified such that the circuit switching call program and the packet switching call program are coupled to a single shared memory.

Second, Kosuge fails to teach a packet switch controller to select an address of a single shared memory for a packet data based on routing data embedded in the packet data and based on the input port which received the packet data. In rejecting claim 21, the Office Action aligns this recited feature with claims 2 and 3 in columns 13-14 of Kosuge. These two claims, however, **fail** to teach, or even fairly suggest, a packet switch controller to select an address of a single shared memory for a packet data based on **routing data embedded in the packet data** and based on the **input port which received the packet data**. Instead, claim 2 of Kosugue claims that the hierarchical storage (item 10 in Figures 1 and 6 of Kosugue) comprises a file memory (item 13 in Figures 1 and 6 of Kosuge) for storing packet switching data corresponding to packet switching calls. Further, claim 3 of Kosugue claims that the hierarchical storage (item 10 in Figures 1 and 6 of Kosugue) is commonly used for a switching program together with the circuit and packet switching calls. **Neither** claim 2 **nor** claim 3 have any teachings related to selecting an address of a single shared memory for a packet data based on routing data embedded in the packet data and based on the input port which received the packet data. Hence, Kosuge fails to teach the recited packet switch controller.

Third, Kosuge fails to inherently teach a time slot interchange controller to select an address of a single shared memory for a TDM data based on a time slot of a frame in which the TDM data was received. In rejecting claim 21, the Office Action correctly asserts that Kosuge

fails to teach the recited time slot interchange controller, but incorrectly asserts that the recited time slot interchange controller is inherently taught by Kosuge. Contrary to this ***inherency*** assertion by the Office Action, Kosuge teaches in Figure 1 switching of circuit data based on **control data extracted** from a **common control channel signal** received by a signal reception circuit 17 from the TDM transmission input lines 15. Kosuge, column 3, line 66, to column 4, line 4. Under control of the processor 18 in Figure 1 of Kosuge, the control section 14 switches TDM data based on the control data extracted from the common control channel signal. Kosuge, column 4, lines 4-6. As illustrated in Figure 2 of Kosuge, the control data extracted from the common control channel signal includes **five data types**: a service indicator A indicating circuit switching or packet switching; a terminal indicator B indicating the terminal type for circuit switching or packet switching; a signal indicator C including supervisory signals, such as an originating signal, a disconnect signal, and an off-hook signal; a rate indicator D including transmission rate data; and a selection data E including a dialing signal. Kosuge, column 4, lines 7-23. **None** of these five data types of Kosuge correspond to selecting an address of a single shared memory for a TDM data based on a **time slot** of a **frame** in which the TDM data was received. Hence, Kosuge fails to teach, inherently teach, or fairly suggest, the recited time slot interchange controller.

Claims 22-26 and 28-30 are dependent from claim 21 and are allowable as being dependent from an allowable claim.

Claim 31 recites limitations similar to those recited for claim 21 and is allowable for reasons similar to those discussed above for claim 21.

Claims 32-33 are dependent from claim 31 and are allowable as being dependent from an allowable claim.

Claim 35 recites limitations similar to those recited for claim 21 and is allowable for reasons similar to those discussed above for claim 21.

Claims 36-40 are dependent from claim 35 and are allowable as being dependent from an allowable claim.

3. Claims 13, 21, 31, 34, and 35 are amended to correct typographical errors and clarify the invention, but not to overcome any claim objections or rejections.

4. Claims 41-53 are added, where claims 41 and 50 are independent claims. Claims 41 and 50 recite limitations similar to those recited for claim 21 and are allowable for reasons similar to those discussed above for claim 21. Claims 42-49 are dependent from claim 41 and are allowable as being dependent from an allowable claim. Claims 51-53 are dependent from claim 50 and are allowable as being dependent from an allowable claim.

5. If no check is attached, or if a greater or lesser fee is required, please charge or credit Deposit Account Number 22-0261 accordingly and notify the undersigned.

THEREFORE, because all objections and rejections have been overcome, it is submitted that claims 13, 21-26, and 28-53 are allowable, and such allowance is requested.

Respectfully submitted,

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